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An adaptive-resolution signal-specific ADC for sensor-interface applications

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Abstract
In this paper, a signal-specific analog-to-digital converter (ADC) with a new structure is proposed, in which the resolution of the ADC is adaptively adjusted by the activity of the input neural signal. The main advantages of the proposed technique for converting sparse and burst-like signals include (1) output data-rate reduction, and (2) power savings in ADC and its succeeding blocks. These benefits are obtained owing to the truncation of bits along in-active part of the signal. The extra blocks for realizing the proposed adaptive-variable resolution technique are fully-digital, which add minimum complexity and design overhead to the ADC. The proposed ADC has a suitable data compression capability at the expense of a tolerable degradation in quality of the reconstructed signal. The simulation results in a 180 nm CMOS technology show power savings of up to 39.5% and a compression ratio of 3.9×, as compared to the conventional structure.

Keywords Data compression · SAR ADC · Signal-dependent behavior · Nonlinear quantization · Biomedical signal

1 Introduction

Nowadays, a wide variety of portable and implantable devices are utilized for diagnostic and therapeutic purposes. We can name a few applications such as monitoring and recording devices, hearing-aid implants, and seizure detection/abruption prosthesis. Also, scientists have developed wearable personal monitoring microsystems, which can wirelessly communicate with the health center, omitting the need for hospitalizing the patients. Furthermore, the development of modern brain-machine interfaces (BMI) has enabled profoundly paralyzed patients to communicate artificially with the outside world by bridging the gap between the patient's motor and sensory systems [1]. These devices process the captured electrophysiological signals from surface or depth of the cortex via wet, dry, and noncontact electrodes. One of the most essential blocks in such a system is the ADC circuitry.

ADCs are essential building blocks operating as interfaces between the physical world and digital signal processors (DSP). ADCs aimed for biomedical applications are usually configured with successive-approximation register (SAR) structure due to its power efficiency. Indeed, low power consumption guarantees a higher battery life and system reliability. Especially, the power sources are extremely constrained in implantable devices and it is usually provided by means of wirelessly rechargeable implanted batteries or power harvesting techniques [2, 3]. In most biomedical applications including body-wearable and implantable devices, a moderate resolution (8–12 bits) and a sampling frequency (hundreds of Hz to tens of KHz) meet desirable system specifications, which can be easily achieved by an SAR ADC [4, 5]. Moreover, the digital switching logic circuitry used in this architecture benefits from technology scaling.

In this paper a signal-specific ADC with activity-dependent adjustable-resolution, which can compress the output digital code and reduce power consumption, is proposed. The paper is organized as follows. Some of the

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state-of-the-art techniques presented for signal-specific digitization are reviewed in Sect. 2. Section 3 describes the principle of the proposed adaptive resolution technique. Section 4 provides simulation results. We finally conclude the paper in Sect. 5.

2 Signal-specific ADCs

The inherent sparse and burst-like nature of some biopotential signals is the main rationale behind the efforts researchers have put on designing signal-specific ADCs [4–11]. Some of these ADCs offer the capability of data compression [4–7]. Generally, when the data compression is embedded in the functionality of the ADC, the power consumption of the ADC and the succeeding DSP can be significantly reduced. Another advantage of this technique is the reduction in data storage and transmission requirements. This is especially of great importance for high-density multi-channel applications and long-term monitoring/recording purposes.

Broadly speaking, the signal-specific ADCs based on the quantization algorithm can be categorized into three main groups:

1. Delta-modulated
2. Asynchronous/Non-uniform sampling
3. Variable resolution

In delta-modulated SAR ADCs, instead of each individual sample, the difference between the amplitudes of two consecutive samples is digitized [10]. This technique results in power savings in digital-to-analog converter (DAC) circuitry, especially for signals with long inactive durations. However, there is a chance of accumulating errors, which can be solved by sampling the incremental value of the input signal as proposed in [11]. Disadvantage of this technique is that preciseness of the output digital code depends on variation of the input signal. In other words, as variation of the input signal increases, effectiveness of this technique may decrease.

For the second category, a sample is generated only when a significant change (i.e., event) occurs in the pattern of the input signal [12–14]. This event can be a variation in the voltage level or slope of the input signal. The clock-less level-crossing (LC) technique is a well-known example of the event-driven ADCs, in which the input signal is sampled when it crosses the specified voltage levels. In the LC technique [15–19], instead of the magnitude of the samples, the time intervals between samples are quantized. Since the intervals between samples vary, they should be digitized using a timer, which can be a counter or an intricate time-to-digital converter (TDC), resulting in a more complexity. Other solutions are the use of continues-time post-processing or generating consecutive samples by a clock to be used in a conventional DSP.

The adaptive sampling structure proposed in [4] is another example of the ADCs in this category, in which to sample the input signal two clock sources with low and high frequencies (f_H and f_L) are used. In this technique, the input signal is permanently monitored by f_H. When the rate of variation of the input signal is low (high), the input signal is sampled by f_L (f_H). Also, to distinguish the time intervals between samples, a 4-bit flag is saved. Although these ADCs benefit from lower power consumption and a reduction of outgoing data rate, the complexity of the circuit increases.

In the last category, the resolution of the ADC is varied to achieve improved functionality [20–25]. Recently, a nonlinear ADC (NLADC) is presented, in which an exponential quantization function is used to map the analog input to the digital code [7]. It is shown that applying a nonlinear quantization function increases the effective resolution and reduces the noise content. The target exponential characteristic is approximated with a piecewise-linear (PWL) curve and then values of capacitors are selected such that this function is realized. To realize the exponential function in [7], capacitors of the DAC should be sized with non-integer values, which may result in increased mismatch between the fractional portions. As another example of the ADCs of the third category, a reconfigurable ADC with a variable resolution (5–10 bits) is designed in [23], which reduces the power consumption of the ADC linearly (exponentially) by reducing voltage (resolution) of the power supply. However, it is not implicitly mentioned that the resolution should be varied based on what condition or signal feature.

In the literature, some ADC structures are presented that employ a combination of the above mentioned techniques [20, 26–28]. These architectures cannot be purely considered in one of the three described categories. For instance, the variable-resolution clock-less converter proposed in [20] has the characteristics of both ADCs in categories 1 and 2. In this structure, when the time between the samples is lower than 40 μs (or higher than 80 μs), the ADC's resolution decreases (or increases) by one bit. Otherwise, the ADC's resolution has been already set at 4 or 8 bits. In this manner, the trade-off between dynamic range and the input bandwidth is optimized. In the clock-less ADCs, a flag should be generated to determine the instant of sampling. However, this issue is not considered in [20] and [26]. Also, decoding data digitized by these ADCs is more complex, as compared to the conventional structure. Thus, the characteristics of the ADC and DSP should be considered together to make a fair comparison between these kinds of ADCs and the conventional one.

3 The proposed adaptive resolution technique

3.1 Principle

Neural signals contain two important components including local field potentials (LFP) and action potentials (AP) [27]. Components of a biomedical signal with a high variation-rate, shown in Fig. 1, can be used for both diagnostic and research purposes. The examples are visual/auditory-evoked potentials or the QRS complex of the electrocardiogram (ECG) signal. Also, seizure onset due to abnormal neural discharges in patients suffering from epilepsy corresponds to sudden high amplitude/frequency spikes in the electroencephalogram (EEG) pattern of these patients. In these cases, low-varying portions of the biomedical signals do not include important information (to be used for seizure onset detection) and also, they may be contaminated with noises. Thus, configuring the ADC with a fixed resolution, in which all signal components are digitized with the same resolution, is not an efficient approach.

3.2 Realization of the variable-resolution ADC

In this section, an SAR ADC with activity-dependent functionality is proposed. The presented structure is designed such that the resolution of the ADC varies based on variation of the input signal. In the proposed structure, inputs with low (high) variations are digitized with lower (higher) resolution. The structure of the proposed variable-resolution ADC (VRADC) is shown in Fig. 2 along with important controlling signals. In the *Reset* (*RS*) phase, DAC capacitors are discharged and the comparator is reset. Also, in the *RS* phase, the input signal is sampled on the capacitors C_s using a bootstrap switch. In the *Slope*

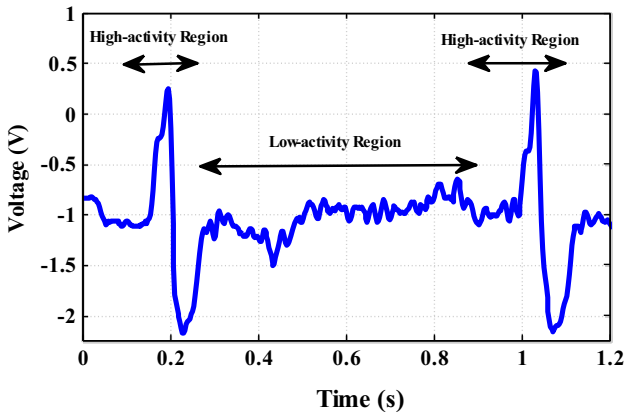

Fig. 1 A typical biopotential signal provided by MIT-BIH database [16]

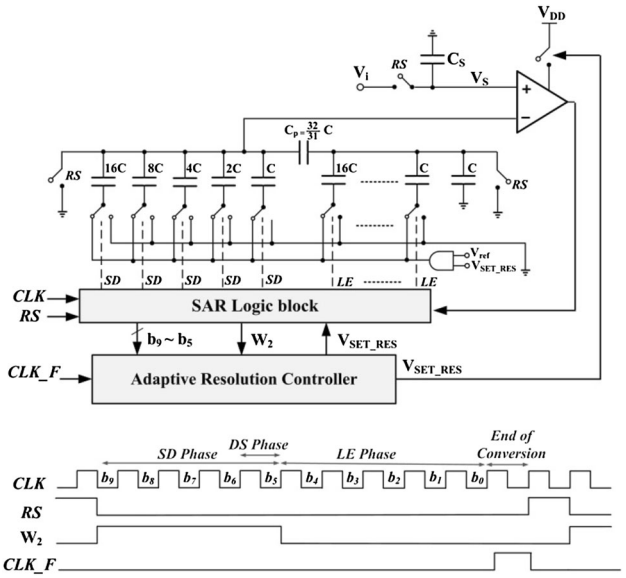

Fig. 2 Structure of the proposed VRADC and the simplified timing diagram

Detection (*SD*) phase, five important MSBs, i.e., $b_9 \sim b_5$ are generated. Then, in the *Decision* (*DS*) phase every sample is compared with the previous one. The logic circuit, shown in Fig. 3(a), decides whether MSBs of the current sample and the previous one are equal or not. To

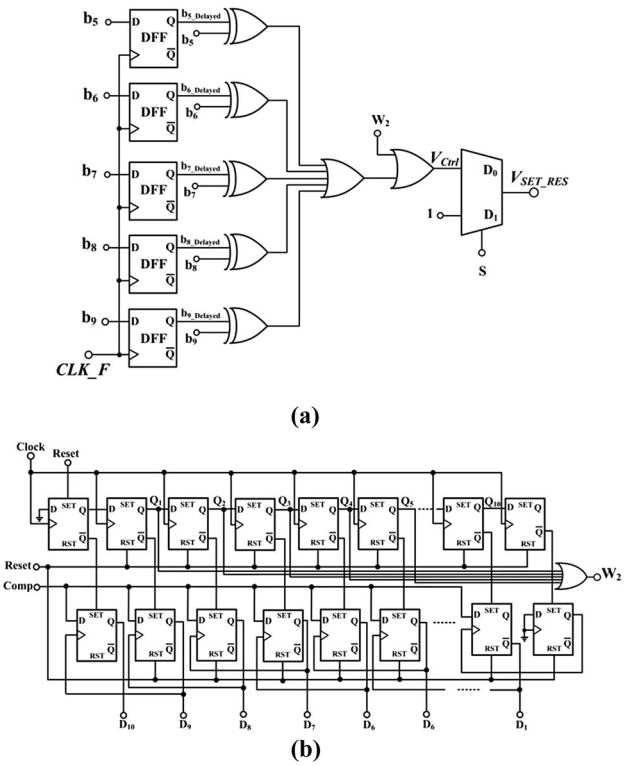

Fig. 3 **a** Schematic of the control logic block for producing V_{Ctrl} signal. **b** Generation of the W_2 signals using $Q_1 \sim Q_5$ signals and an *OR* gate

make the comparison in the digital domain, MSBs of the previous sampled data is saved in D-flip-flops to be used in the succeeding phase.

Principle of the proposed technique is based on the fact that if absolute difference of two analog voltages (to be digitized with M bits) is higher than 2^K bits, the $(M-K)$ MSBs of their corresponding digital codes are not equal. As a sample implementation of the proposed technique, a logic circuit is employed to compare five MSBs of the current sample and the previous one (Fig. 3a). If absolute difference of the samples (called D_S) is higher than $\frac{V_{ref}}{2^5}$ (32 LSB), outputs of the XOR gates become one. Generally, if K XOR gates are used in the ADC with M-bit resolution, D_S is set to $\frac{V_{ref}}{2^K}$ which equals 2^{M-K} LSB. Usually, in approaches that diagnose activity of the signal, such as those presented in [5] and [13], analog blocks (e.g., differentiator, comparator, and timer) are used. But in the proposed adaptive-variable resolution controller, shown in Fig. 3(a), all of blocks are digital, which indeed benefits from technology scaling and lower complexity.

As illustrated in Fig. 2, at the end of the conversion phase, *CLK_F* signal becomes high and hence, five MSBs of the current sample are registered in D-flip flops to be used for the *comparison* in the next conversion phase. Since the calculated bits are registered in flip-flops of the control logic block up to the end of every conversion phase, outputs of the XOR gates remain valid until that time and they can be used for activating the comparator during the *LSB Estimation* (*LE*) phase. As seen in Fig. 3(a), the W_2 signal is used in the control logic block to activate the comparator during the *SD* phase, in which five MSBs are generated. Also, the W_2 signal is generated by applying outputs of the upper flip-flops illustrated in Fig. 3(b) ($Q_1 \sim Q_2$) to an *OR* gate. As seen in Fig. 3, a selector (the S signal) provides the opportunity to configure the ADC in the adaptive resolution mode ($S = 0$) or in the fixed-resolution mode ($S = 1$). Finally, V_{SET_RES} signal is used for activating comparator of the SAR ADC.

The V_{Ctrl} signal is always high in the *SD* phase and it may be high (low), if MSBs of the samples are equal (unequal) in the *LE* phase. By applying this signal to the comparator, its resolution can be adjusted according to the variation rate of the input signal. Considering the configuration shown in Fig. 3, resolution of the VRADC is set to 5 (10) bits if MSBs of the samples are equal (unequal). Accordingly, the comparator is turned off during the *LE* phase for input signals with a low activity, resulting in power savings. On the other side, the comparator is activated during the *LE* phase for high-activity inputs. The more bits (per each sample) are generated, the more power the SAR segment consumes. In order to save power in the SAR ADC, the V_{SET_RES} signal is used to turn SAR ADC blocks off. The lower resolution, the less time period SAR ADC should be activated.

Usually in adaptive sampling techniques, a flag signal is generated which is used for regenerating the analog input signal and further processing in DSP. In the proposed structure, the V_{Ctrl} signal can be considered as the flag signal. For achieving the highest compression capability, when $V_{Ctrl} = 0$, only the flag signal is considered as the digital code of the sample. In other word, for reconstructing the digitized signal in the DSP platform, when the flag signal is zero, the digital code corresponding to previous sample is used as the digital code of the current sample.

To investigate behavior of the designed ADC in the transient mode, the biomedical signal shown in Fig. 1 is applied to the ADC. As seen in Fig. 4(a), the V_{Ctrl} signal becomes one (zero), when activity of the input signal is high (low). The original and reconstructed signals are shown in Fig. 4(b). Figure 4(c) depicts the quantization function. Regarding to Fig. 4(c), the quantization noise (Q-Noise) becomes maximum (minimum), when input activity is low (high). This noise becomes near zero along the action potential part. In contrast, the Q-Noise contains input noise along in-active part of the signal, which means that the output data volume does not contain non-useful noisy part of the signal. Maximum of the Q-Noise can be calculated by

$$\mathrm{Q-Noise_{Max}} = \pm 2^{M-K} \times \mathrm{V_{LSB}} \quad (1)$$

in which M and K are resolution of the VRADC and number of the XOR gates employed in the control logic block, respectively. Also, V_{LSB}, which is the smallest voltage can be detected by the ADC, equals $\frac{V_{ref}}{2^M}$. For instance, if we consider $M = 10$ and $K = 5$, maximum value of the Q-Noise, evaluated by (1), is ± 31.25 mV. This issue can be observed in Fig. 4(c), as well.

To study effect of the variation of K on quality of the reconstructed signal, we have applied the ECG record number 118 provided by the Arrhythmia MIT-BIH database to the designed VRADC. The reconstructed signal using first-order interpolation for different values of K is depicted in Fig. 5(a). As can be observed from this Figure, quality of the reconstructed signal decreases as K increases. However, this issue is observed along inactive and noisy parts of the signal, rather than the action potential part. Furthermore, the quantization noises versus time for $K = 3$ and $K = 6$ are illustrated in Fig. 5(b). Regarding (1), it can be concluded that the Q-Noise decreases by a factor of 8, when K increases from 3 to 6 bits. Reduction of the Q-Noise by increasing K can be observed in Fig. 5(b) as well.

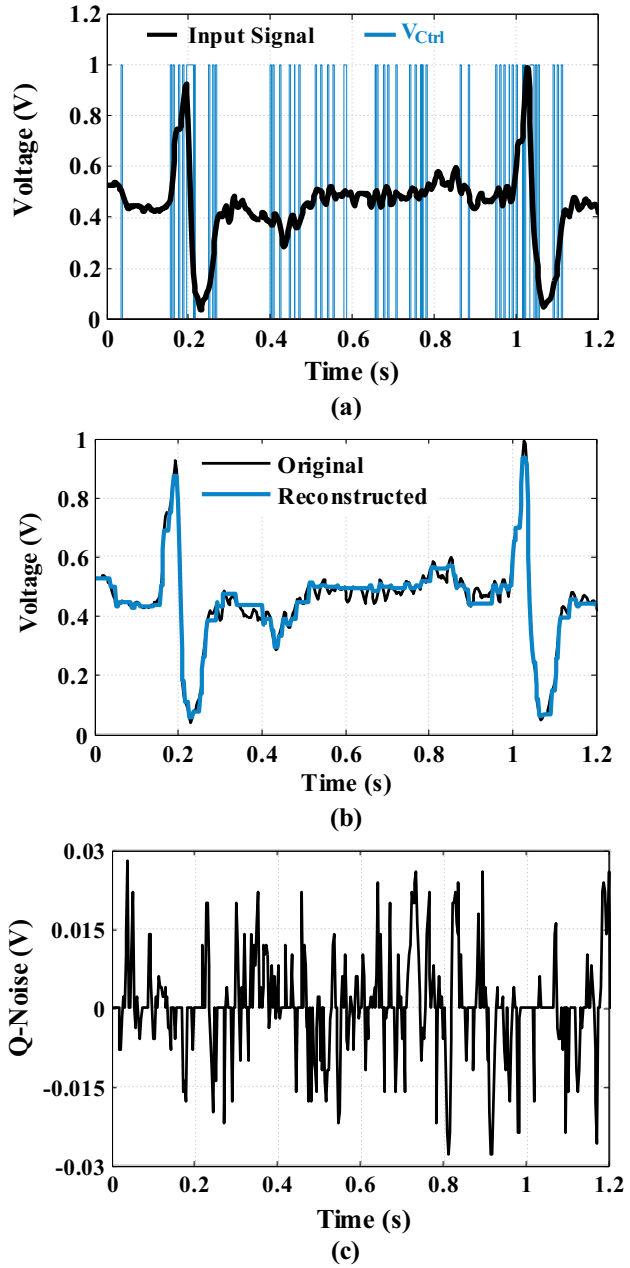

Fig. 4 Record number 118 of the MIT-BIH database. **a** The V_{Ctrl} signal, **b** original and recovered signals, **c** quantization noise versus time

3.3 Data compression capability

As mentioned before, one of the advantages of the proposed technique is reduction of the output data volume. To asses data compression capability of an ADC, a merit called the compression ratio (*CR*), is defined. The parameter *CR* is ratio of the output data without using any compression technique to the compressed output data. The value of the *CR* can be calculated by

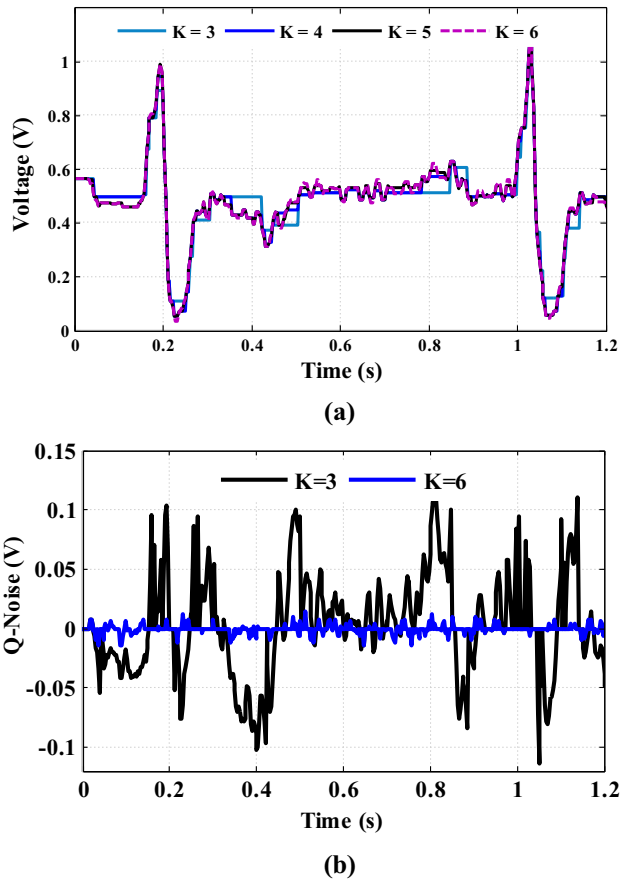

Fig. 5 **a** Reconstructed signal when signal shown in Fig. 1 is applied to the proposed VRADC. **b** Q-Noise for different values of *K* versus time

$$CR = \frac{N_{\text{Sample}} \times M}{N_1 \times K_{\text{Flag}} + N_2 \times (M + K_{\text{Flag}})} = \frac{N_{\text{Sample}} \times 10}{N_1 \times 1 + N_2 \times (11)} \quad (2)$$

where N_1 and N_2 are numbers of the samples corresponding to the condition if MSBs of the samples are equal or unequal, respectively. Also, sum of the N_1 and N_2 samples equals N_{Sample}, which is total number of the samples. Moreover, M is the full resolution of the ADC and K_{Flag} is the number of the bits considered for the flag signal. Regarding (2), value of the *CR* depends on waveform of the input signal. As a test input, we applied the biopotential signal illustrated in Fig. 1 to the ADC. The parameters are as follows

$$N_{\text{Sample}} = 613, \quad N_1 = 375, \quad N_2 = 238 \quad (3)$$

Substituting parameters given in (3)–(2) yields $CR = 2.04$, which means that the memory size for recording this signal is reduced to 49%.

As seen in Fig. 1, a typical AP has a sparse and burst-like nature and it may experience long inactive durations.

This means that number of the samples to be digitized with a low resolution is much higher than those to be digitized with a high resolution. Hence, we can conclude

$$N_2 \ll N_1 \quad \text{and} \quad N_{\text{Sample}} \cong N_1 \tag{4}$$

Accordingly, maximum of the *CR* can be found as

$$CR_{\text{Max}} = \frac{N_{\text{Sample}} \times 10}{N_1 \times 1} \cong 10 \tag{5}$$

Regarding (5), the *CR* value is limited to 10 in theory. If number of MSBs of the samples to be compared is selected lower, the *CR* value calculated by (3) increases; however, at the expense of the lower precision at medium variation rates. To address this issue numerically, usually a parameter called percentage root-mean-square difference (*PRD*), is calculated as follows [28]

$$PRD = \frac{||\mathrm{X} - \tilde{\mathrm{X}}||_2}{||\mathrm{X}||_2} \times 100 \tag{6}$$

in which X and $\tilde{X}$ are vectors of the original and reconstructed signals, respectively. As a numerical example, the calculated value of the *PRD* for the signal depicted in Fig. 1, when applied to the designed VRADC, equals 4.47%. As stated in [28], a *PRD* less than 9% determines that the reconstructed signal has a "good" or "very good" quality.

3.4 Power savings capability

By setting the resolution as described, the SAR SDC is (activated) deactivated during the in-active (active) part of the input signal, which corresponds to N_1 (N_2) samples. Hence, for a high percentage of the samples (N_2 samples), the SAR ADC is deactivated. Accordingly, η_{power} which is ratio of the power consumption of the proposed structure,$P_{\text{Prop.}}$, to that of the conventional one, $P_{\text{Conv.}}$, can be calculated by

$$\eta_{\text{Power}} = \frac{P_{\text{Prop.}}}{P_{\text{Conv.}}} = \frac{\frac{N_1}{N_{\text{Sample}}} \times P_{\text{SAR\_5b}} + \frac{N_2}{N_{\text{Sample}}} \times (P_{\text{SAR\_10b}})}{P_{\text{SAR\_10b}}} \tag{7}$$

where $P_{\text{SAR\_5b}}$ and $P_{\text{SAR\_10b}}$ are power consumptions of the SAR ADC with a resolution of 5 bits and 10 bits, respectively. Considering (7), we can conclude

$$\eta_{\text{Power}} \cong \frac{N_2}{N_{\text{Sample}}} < 1 \tag{8}$$

Thus, considering (8), we can conclude that the proposed structure is power-efficient.

3.5 Circuit's components

Since variation of the input biomedical signal and hence, output bit rate are not high, flip-flops are configured with a static structure. Also, schematic diagram of the comparator employed in the SAR ADC is depicted in Fig. 6. As seen in Fig. 6, the employed dynamic comparator includes a NAND-based regenerative latch. Transistor sizing of the employed double-tail dynamic comparator is reported in Table 1. Open-loop gain of the employed comparator is 65 dB. If a comparator with a higher gain is utilized, the quantization error decreases which results in a higher signal-to-quantization-noise ratio (*SQNR*).

4 Simulation results

As a case study, a SAR ADC is designed in the standard 180 nm CMOS technology to evaluate the functionality of the proposed technique. We have applied ECG records provided by the Arrhythmia MIT-BIH database [29] to the ADC. It is assumed that these signals have been amplified with a sufficient gain to cover the full-scale range ($0 \sim V_{\text{DD}}$). Usually, these amplifiers block the electrodes' offset and set the DC bias point of the output to $V_{\text{DD}}/2$. Hence, we can assume that the baseline voltage of the input signal applied to the ADC equals $V_{\text{DD}}/2 = 0.5V$.

In order to study the effect of increasing D_{S} on characteristics of the designed VRADC, *CR* and *PRD* parameters are evaluated for different configurations. Results are reported in Table 2. Based on these results, D_{S} and *CR* are in a direct relation. The reason is that for a higher D_{S} number of the samples with the same MSBs increases and more samples are digitized with only one bit. However, this benefit is achieved at the expense of a higher *PRD*. Regarding the data reported in Table 2, the proposed VRADC has a suitable data compression capability at the expense of a tolerable degradation in the signal quality. It is apparent that the former, which is the achievement, is more important than the latter, which is the penalty paid. Note that the *PRD* parameter is less than 9% for all cases.

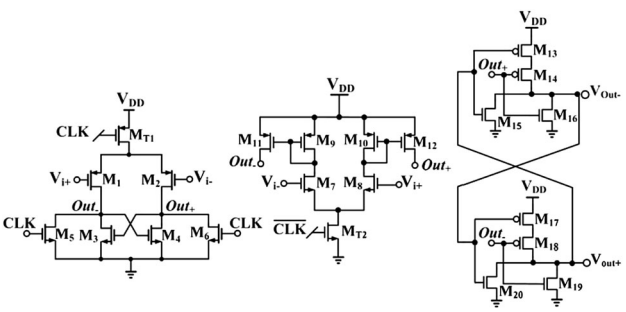

Fig. 6 Double-tail dynamic comparator with a regenerative latch

Table 1 Dimension of transistors for realizing double-tail comparator

Transistor	M_{T1}	M_{T2}	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$
W/L (μm/μm)	1/0.4	1/0.4	1/0.36	1/0.3	1/0.2
Transistor	$M_{7,8}$	$M_{9,10}$	$M_{11,12}$	$M_{13,14}$ and $M_{17,18}$	$M_{15,16}$ and $M_{19,20}$
W/L (μm/μm)	1/0.3	3/0.6	2/0.6	3/0.18	1/0.18

Table 2 *CR* and *PRD* values as a function of *D*s for the record number 118 shown in Fig. 1

*D*s (LSB)	*K*	N_1	N_2	*CR*	*PRD* (%)
128	3	545	68	4.68	8.81
64	4	483	130	3.18	4.47
32	5	377	236	2.04	1.96
16	6	260	353	1.48	0.76

Assuming a fixed resolution of 10 bits per sample, 38.9 Mbytes of the memory is required for recording the ECG of a patient for 1 day. Record number 234 provided by MIT-BIH database is a regular ECG signal without any abnormality. Assuming $D_S = 32\,LSB$ for this signal, the *CR* parameter equals 2.04. Hence, if the proposed technique is employed in the ADC, the required mentioned memory size reduces from 38.9 to 13.41 Mbytes. In order to evaluate the variations of *CR* versus D_S (Fig. 7), we calculate *CR* for four random samples provided by the MIT-BIH database, when D_S is 16, 32, 64, and 128 LSB. Then, for each random sample a line is passed through four pieces of data. To set D_S equal to 16, 32, 64, and 128 LSB, we have used 6, 5, 4, 3 XOR gates in the control logic block (shown in Fig. 3a), respectively. For these cases *PRD* is calculated and drawn in Fig. 8. According to Fig. 7, *CR* varies approximately from 2 to 6 when D_S changes from 16 LSB to 128 LSB. Regarding Fig. 8, for records number 100 and 234, *CR* should be limited to less than 4 to achieve suitable quality ($PRD < 9\%$).

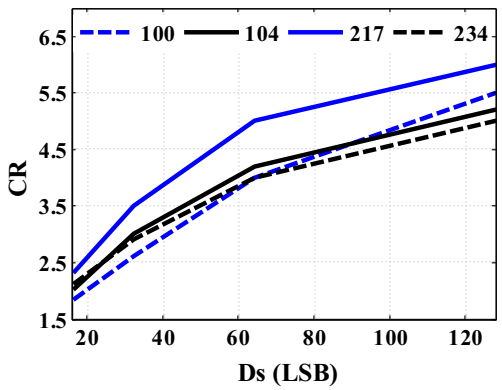

Fig. 7 Variation of *CR* versus D_S for different input signals

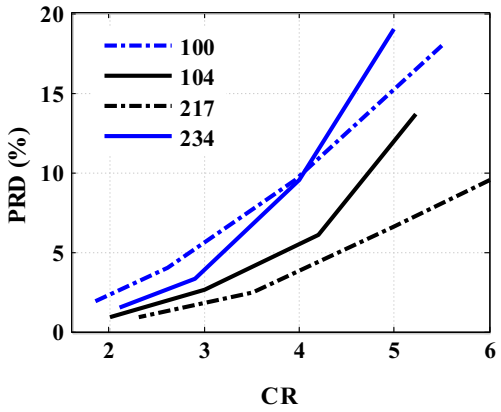

Fig. 8 Variation of *PRD* versus *CR* for random input signals

The output data bit size of the ADC is the sum of resolution of the ADC and the flag bit. When the Flag is one (zero) the ADC is activated (deactivated), which means that the data bit size is (1) 11. In other words, the output digital volume representing each sample can be 1 or 11 bits and it can vary according to activity of the input signal. Figure 9 illustrates the digital codes corresponding to four analog input examples, which are digitized by the conventional ADC and the proposed VRADC. As can be observed from Fig. 9, the flag signal becomes 1 (0) in the proposed VRADC, when five MSBs of two succeeding analog input signals are different (the same). Hence, the length of the output digital word is 11 (1) in the mentioned cases.

Figure 10 shows the power consumption of the SAR ADC comparator versus its resolution for different power supply voltages. As can be inferred from this Figure, the

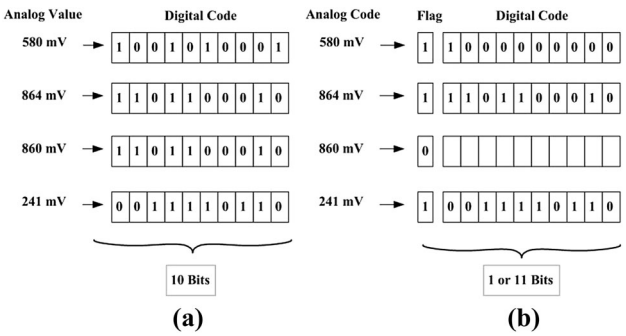

Fig. 9 Illustration of digitization using **a** Conventional linear ADC. **b** The proposed VRADC

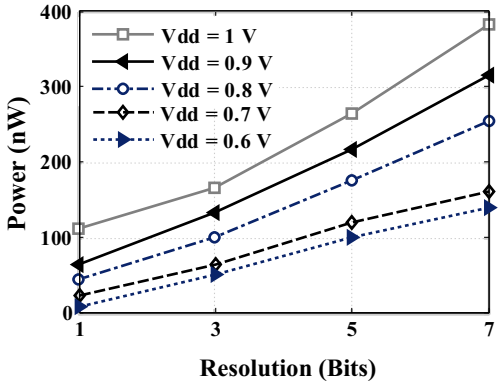

Fig. 10 Power consumption of the SAR ADC comparator versus its resolution

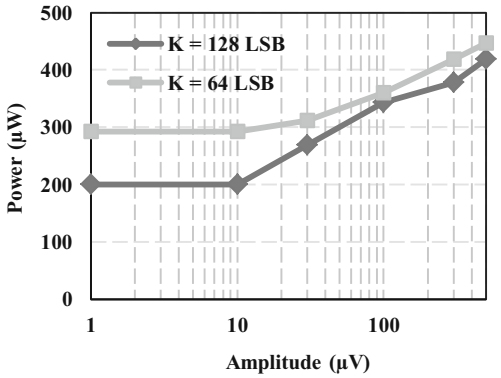

Fig. 12 Power consumption as a function of input amplitude ranging from 1 to 500 mV for input frequency of 100 Hz

power consumption decreases significantly by reducing the resolution of the ADC. For instance, when resolution of the SAR ADC decreases from 7 bits to 1 bit (V_{DD} = 1 V), the power reduces by 3.38×. Hence, the proposed adaptive-variable resolution technique can lead to power savings in the comparator block, which is the most power hungry component.

Power contribution of different blocks of the designed VRADC is illustrated in Fig. 11. This simulation is carried out when V_{DD} is set at 1 V and the ADC's resolution is 10 bits. Regarding this Figure, the most and the least percentages of the power budget are consumed by the comparator of the SAR ADC and the capacitive DAC, respectively. Furthermore, power consumption of the comparator versus amplitude of the input sinusoidal voltage is illustrated in Fig. 12. Regarding this figure, higher power consumptions correspond to higher input amplitudes. Also, the ADC consumes more power when K decreases. The reason is that for higher values of K the V_{Ctrl} signal remains high for more number of the samples, which

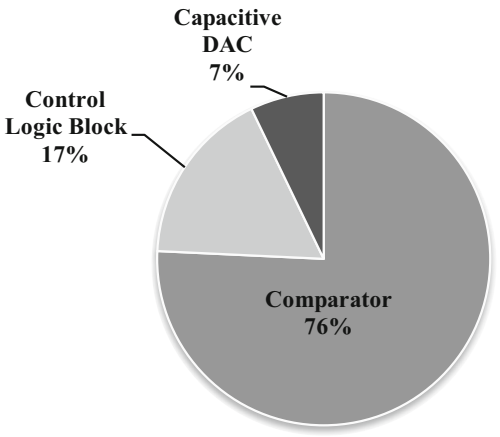

Fig. 11 Pie diagram of the power distribution in the designed VRADC

in turn causes drawing more current from the supply voltage.

Assuming a fixed resolution of 10 bits per sample, a memory with size of 38.9 Mbyte is required for recording one-day ECG of a patient. Record number 234 provided by MIT-BIH database is a regular ECG signal without abnormality. By applying this signal to the designed VRADC a *CR* equal to 3.9 is achieved. Hence, if the proposed technique is employed in the ADC, the mentioned memory size reduces from 38.9 to 9.97 Mbyte. These values are summarized in Table 3 as well. As reported in this Table, the average power consumption of the proposed VRADC over one normal ECG period is 39.5% less than that of a conventional ADC.

Figure 13 illustrates sampling clock, V_{Ctrl}, V_{Comp}, as well as the currents taken from V_{ref} (I_{DAC}) and the comparator (I_{Copm}) during three sampling periods (T_1, T_2 and T_3). Since during the T_1 and T_3 intervals difference between current sample and the previous one (D_S) is higher than 32 LSB, the V_{Ctrl} signal becomes one during whole of the conversion period. However, during T_2 interval D_S is less than 32 LSB, which in turn causes deactivating the comparator and DAC circuitry for five clock cycles. It is apparent when V_{Ctrl} becomes zero, the currents consumed by the comparator and DAC become zero. Note that for a sparse signal with long inactive durations this condition accrues for most of the time.

In order to verify the performance of the circuit, it is simulated at all process corners. The power consumption is evaluated at different process corners, including Fast Fast (FF), Fast Slow (FS), Slow Fast (SF), and Slow Slow (SS). Also, three supply voltages (0.9, 1, and 1.1 V) are applied to the ADC. The simulation results are illustrated in Fig. 14. According to Fig. 14, the most and least power consumptions correspond to FF-1.1 V and SS-0.9 V, respectively. As seen in Fig. 14, power consumption increases as voltage of the power supply increases. Layout of the designed ADC is illustrated in Fig. 15.

Table 3 Comparison of the characteristics of the proposed VRADC with the conventional ADC in 180 nm technology node

Parameters	Conventional ADC	Proposed VRADC
V_{DD}	1 V	1 V
Sampling Frequency (S/s)	5 k	5 k
Data size (Bit)	10	1 or 11
CR	1	Up to 3.89 (depending on the input signal)
Memory storage needed for 1-day recording	38.9 Mbyte	8.64 Mbyte
Normalized average power consumption	1	0.60

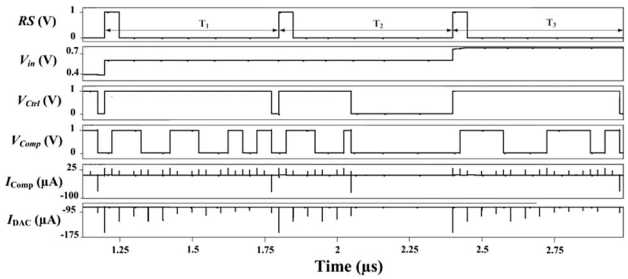

Fig. 13 Waveforms of the important nodes of the designed VRADC

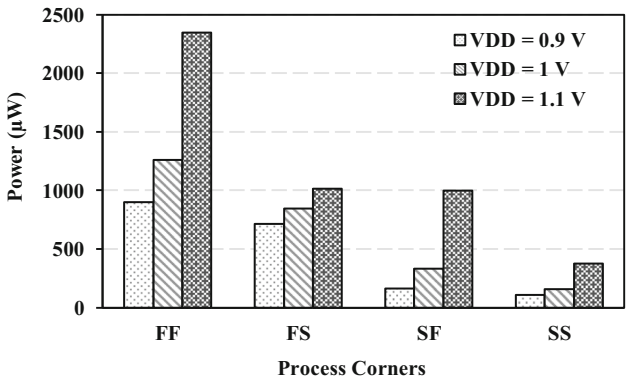

Fig. 14 Power consumption of the ADC at different process corners and supply voltages

Table 4 compares characteristics of this work with some state-of-the-art works. As reported in this Table, the proposed signal-specific VRADC has a good compression capability, while it consumes the least power as compared with other adaptive techniques. The average power consumption reported in Table 4 is calculated over one period of the signal depicted in Fig. 1 and also, when D_S is assumed to be 128 LSB. As reported in Table 4, the ADC provides a *SQNR* equal to 57.59 dB and differential and integral nonlinearities (*DNL* and *INL*) equal to 0.6 LSB and 1.5 LSB, respectively. Moreover, when ADC operates in the 10-bit resolution mode, it achieves an effective number of bits (*ENOB*) of 9.3 bits, which in turn yields a figure of merit (*FOM*) [11] equal to 126.9 fJ/Conversion. It is worth noting that input range of the signal in terms of voltage and frequency are 1 V and 2 KHz, respectively.

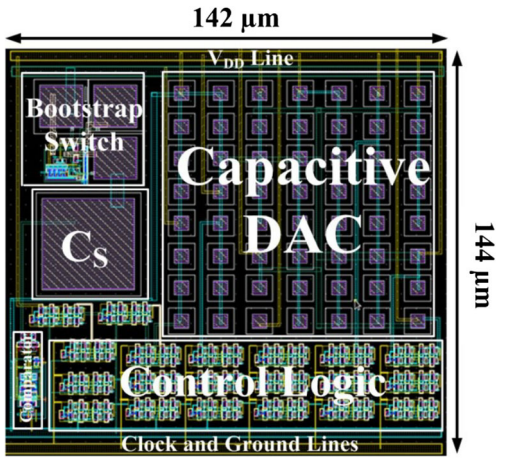

Fig. 15 Layout of the proposed VRADC with the area of 142 µm × 144 µm

5 Conclusion

A power-efficient structure with low complexity is proposed in this paper, which compresses the output digital data. The adaptive-variable resolution technique embedded in the ADC quantization function reduces the resolution along the in-active part of the input signal. In contrast, components with a high variation, which convey important information, are digitized with the highest precision. This technique is realized using a SAR ADC circuit structure, which results in power savings and output data rate compression. Circuit level simulations in 180 nm CMOS technology demonstrates that using the proposed technique in the ADC circuitry results in 39.5% power savings and 3.9× compression ratio. Lower power consumption and less design complexity have been achieved due to the proposed topology. Total memories required for 1-day

Table 4 Comparison of ADCs' characteristics

Parameter	[4]	[5]	[7]	This work
Architecture	Adaptive sampling	Adaptive sampling	Nonlinear signal-specific	Variable resolution
Technology (nm)	180	500	180	180
V_{DD} (V)	1	2	1	1
Sampling rate (*S/s*)	1.33 k	64/1024	25 k	5 k
Power (μW)	0.54	5.2	87.2	0.420
Maximum resolution (Bit)	10	11	8	10
Data size (Bit)	14	11	3 ∼ 8	1 or 11
CR	7.5	7	1.21	3.89
PRD (%)	2.67	NA	NA	4.5
SQNR (dB)	NA	NA	NA	57.59
Area (μm^2)	90,832	723,600	36,000	20,448
INL (LSB)	NA	NA	4.3/-2.1	1.5
DNL (LSB)	NA	NA	0.8/-0.9	0.6
FOM (fJ/Conv.)	NA	NA	2403[a]	126.9
Sim./Meas.	Sim.	Meas.	Meas.	Sim.

[a]Since FOM was not reported in [7] we have calculated by using the values reported for power, sampling frequency and *ENOB* in [7]

recording in conventional and the proposed systems are 38.9 and 9.97 Mbyte, respectively.

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